What is claimed is:

1. A doped aluminum oxide layer, comprising:
an aluminum oxide layer having pores on a surface; and
a dopant material filling the pores;
wherein the dopant material is selected from the group consisting of silicon, zirconium, hafnium and titanium; and
wherein the dopant material is applied to the aluminum oxide layer subsequent to a formation of the aluminum oxide layer such that the dopant material is not dispersed throughout the aluminum oxide layer.

2. The doped aluminum oxide layer of claim 1, wherein the aluminum oxide layer further includes voids below the surface and wherein the voids are free of the dopant material.

3. The doped aluminum oxide layer of claim 1, wherein the aluminum oxide layer is formed by a method selected from the group consisting of thermal evaporation, electron-beam evaporation and ion-beam-assisted deposition.

4. The doped aluminum oxide layer of claim 3, wherein a degree of porosity of the aluminum oxide layer is controlled during formation of the aluminum oxide layer using a method selected from the group consisting of ion bombardment and plasma activation.

5. The doped aluminum oxide layer of claim 3, wherein a degree of porosity of the aluminum oxide layer is controlled by bombarding the surface of the aluminum oxide layer with oxygen ions during formation.

6. The doped aluminum oxide layer of claim 1, wherein the aluminum oxide layer has a packing density between approximately 0.65 and 0.999.

7. The doped aluminum oxide layer of claim 1, wherein the aluminum oxide layer has a packing density between approximately 0.85 and 0.999.

8. The doped aluminum oxide layer of claim 1, wherein the dopant material constitutes approximately 0.1% to 30% by weight of the doped aluminum oxide layer.

9. The doped aluminum oxide layer of claim 1, wherein the dopant material constitutes approximately 0.1% to 10% by weight of the doped aluminum oxide layer.

10. The doped aluminum oxide layer of claim 1, wherein the aluminum oxide layer has a degree of porosity such that the dopant material filling the pores of the aluminum oxide layer constitutes approximately 0.1% to 30% by weight of the doped aluminum oxide layer.

11. The doped aluminum oxide layer of claim 1, wherein the aluminum oxide layer has a degree of porosity such that the dopant material filling the pores of the aluminum oxide layer constitutes approximately 0.1% to 10% by weight of the doped aluminum oxide layer.

12. The doped aluminum oxide layer of claim 1, wherein the dopant material is blanket deposited on the aluminum oxide layer.

13. The doped aluminum oxide layer of claim 12, wherein excess dopant material is removed from the surface of the aluminum oxide layer.

14. The doped aluminum oxide layer of claim 13, wherein removing the excess dopant material comprises exposing the excess dopant material to an ion beam.

15. The doped aluminum oxide layer of claim 14, wherein exposing the excess dopant material to an ion beam further comprises exposing the excess dopant material to a beam of argon ions.

16. The doped aluminum oxide layer of claim 12, wherein the dopant material is silicon formed by a chemical vapor deposition using dilute silane in nitrogen and a substrate temperature of approximately 300°C to 350°C.

17. The doped aluminum oxide layer of claim 12, wherein the dopant material is deposited to a thickness less than or equal to an average diameter of the pores.

18. A doped aluminum oxide layer, comprising:

an aluminum oxide layer having pores on a surface, wherein the aluminum oxide layer is formed using an evaporation physical vapor deposition technique; and

a dopant material filling the pores;

wherein the dopant material is selected from the group consisting of silicon, zirconium, hafnium and titanium; and

wherein the dopant material is applied to the aluminum oxide layer subsequent to a formation of the aluminum oxide layer such that the dopant material is not dispersed throughout the aluminum oxide layer.

19. The doped aluminum oxide layer of claim 18, wherein a degree of porosity of the aluminum oxide layer is controlled during formation of the aluminum oxide layer using a method selected from the group consisting of ion bombardment and plasma activation.

20. The doped aluminum oxide layer of claim 18, wherein the aluminum oxide layer has a packing density between approximately 0.65 and 0.999.

21. The doped aluminum oxide layer of claim 18, wherein the dopant material constitutes approximately 0.1% to 10% by weight of the doped aluminum oxide layer.

22. The doped aluminum oxide layer of claim 18, wherein the aluminum oxide layer has a degree of porosity such that the dopant material filling the pores of the aluminum oxide layer constitutes approximately 0.1% to 30% by weight of the doped aluminum oxide layer.

23. The doped aluminum oxide layer of claim 18, wherein the dopant material is blanket deposited on the aluminum oxide layer.

24. The doped aluminum oxide layer of claim 23, wherein excess dopant material is removed from the surface of the aluminum oxide layer.

25. The doped aluminum oxide layer of claim 23, wherein the dopant material is deposited to a thickness less than or equal to an average diameter of the pores.

26. A dielectric layer, comprising:
an aluminum oxide layer having pores on a surface; and
a second dielectric material embedded in the pores of the aluminum oxide layer;
wherein the second dielectric material is formed of a dopant material selected from the group consisting silicon, zirconium, hafnium and titanium; and
wherein the dopant material is embedded in the pores of the aluminum oxide layer after formation of the aluminum oxide layer, such as not to disperse the dopant material throughout the aluminum oxide layer, and the dopant material is subsequently converted to a dielectric form selected from the group consisting of an oxide form and a nitride form.

27. The dielectric layer of claim 26, wherein the aluminum oxide layer further contains voids below the surface and wherein the voids are free of the second dielectric material.

28. The dielectric layer of claim 26, wherein the aluminum oxide layer is formed by a method selected from the group consisting of thermal evaporation, electron-beam evaporation and ion-beam-assisted deposition.

29. The dielectric layer of claim 28, wherein a degree of porosity of the aluminum oxide layer is controlled during formation of the aluminum oxide layer using a method selected from the group consisting of ion bombardment and plasma activation.

30. The dielectric layer of claim 28, wherein a degree of porosity of the aluminum oxide layer is controlled by bombarding the surface of the aluminum oxide layer with oxygen ions during formation.

31. The dielectric layer of claim 26, wherein the aluminum oxide layer has a packing density between approximately 0.65 and 0.999.

32. The dielectric layer of claim 26, wherein the aluminum oxide layer has a packing density between approximately 0.85 and 0.999.

33. The dielectric layer of claim 26, wherein the dopant material embedded in the pores constitutes approximately 0.1% to 30% by weight of the dielectric layer.

34. The dielectric layer of claim 26, wherein the dopant material embedded in the pores constitutes approximately 0.1% to 10% by weight of the dielectric layer.

35. The dielectric layer of claim 26, wherein the aluminum oxide layer has a degree of porosity such that the dopant material embedded in the pores constitutes approximately 0.1% to 30% by weight of the dielectric layer.

36. The dielectric layer of claim 26, wherein the aluminum oxide layer has a degree of porosity such that the dopant material embedded in the pores constitutes approximately 0.1% to 10% by weight of the dielectric layer.

37. The dielectric layer of claim 26, wherein the dopant material is blanket deposited on the aluminum oxide layer and subsequently treated to convert the dopant material to its dielectric form.

38. The dielectric layer of claim 37, wherein excess dopant material is removed from the surface of the aluminum oxide layer prior to converting the dopant material to its dielectric form.

39. The dielectric layer of claim 38, wherein removing the excess dopant material comprises exposing the excess dopant material to an ion beam.

40. The dielectric layer of claim 39, wherein exposing the excess dopant material to an ion beam further comprises exposing the excess dopant material to a beam of argon ions.

41. The dielectric layer of claim 37, wherein the dopant material contains silicon formed by a chemical vapor deposition using dilute silane in nitrogen and a substrate temperature of approximately 300°C to 350°C, and wherein the silicon of the dopant material is converted to silicon dioxide using rapid thermal annealing in an oxygen-containing atmosphere.

42. The dielectric layer of claim 37, wherein the dopant material is deposited to a thickness less than or equal to an average diameter of the pores.

43. The dielectric layer of claim 26, wherein the dielectric layer is a gate dielectric layer of a field-effect transistor.

44. The dielectric layer of claim 26, wherein the dielectric layer is an intergate dielectric layer of a floating-gate field-effect transistor.

45. The dielectric layer of claim 26, wherein the dielectric layer is a capacitor dielectric layer of a capacitor.

46. A field-effect transistor, comprising:

a gate stack overlying a substrate, wherein the gate stack includes a gate dielectric layer having an aluminum oxide layer and a second dielectric material embedded in a surface of the aluminum oxide layer, wherein a dopant material is embedded in the surface of the aluminum oxide layer after a formation of the aluminum oxide layer, thereby not dispersing the dopant material throughout the aluminum oxide layer, and the dopant material is subsequently treated to form the second dielectric material, and wherein the dopant material is selected from the group consisting of silicon, zirconium, hafnium and titanium;

a first source/drain region in the substrate adjacent a first sidewall of the gate stack; and

a second source/drain region in the substrate adjacent a second sidewall of the gate stack.

47. The field-effect transistor of claim 46, wherein the field-effect transistor is an access transistor for a memory cell of a dynamic random access memory device.

48. The field-effect transistor of claim 46, wherein the field-effect transistor is a floating-gate field-effect transistor.

49. The field-effect transistor of claim 48, wherein the floating-gate field-effect transistor is a flash memory cell of a flash memory device.

50. The field-effect transistor of claim 46, wherein the second dielectric material is a dielectric material selected from the group consisting of oxide forms of silicon, zirconium, hafnium and titanium, and nitride forms of silicon.

51. The field-effect transistor of claim 46, wherein the second dielectric material is a dielectric material selected from the group consisting of silicon dioxide, zirconium dioxide, hafnium dioxide, titanium dioxide and silicon nitride.

52. The field-effect transistor of claim 46, wherein the aluminum oxide layer is formed by a method selected from the group consisting of thermal evaporation, electron-beam evaporation and ion-beam-assisted deposition.

53. The field-effect transistor of claim 52, wherein a degree of porosity of the aluminum oxide layer is controlled during formation of the aluminum oxide layer using a method selected from the group consisting of ion bombardment and plasma activation.

54. The field-effect transistor of claim 46, wherein the aluminum oxide layer has a packing density between approximately 0.66 and 0.999.

55. The field-effect transistor of claim 46, wherein the dopant material constitutes approximately 0.1% to 30% by weight of the gate dielectric layer.

56. The field-effect transistor of claim 46, wherein the aluminum oxide layer has a degree of porosity such that the dopant material embedded in the surface of the aluminum oxide layer constitutes approximately 0.1% to 30% by weight of the gate dielectric layer.

57. The field-effect transistor of claim 46, wherein dopant material is formed by blanket depositing the dopant material on the surface of the aluminum oxide layer.

58. The field-effect transistor of claim 57, wherein excess dopant material is removed from the surface of the aluminum oxide layer prior to treating the dopant material.

59. The field-effect transistor of claim 57, wherein the second dielectric material contains silicon dioxide formed by a chemical vapor deposition of silicon using dilute silane in nitrogen and a substrate temperature of approximately 300°C to 350°C, followed by rapid thermal annealing the silicon in an oxygen-containing atmosphere.

60. The field-effect transistor of claim 57, wherein the dopant material is deposited to a thickness less than or equal to an average diameter of the pores.

61. A floating-gate field-effect transistor, comprising:

a gate stack overlying a substrate, wherein the gate stack includes a control-gate layer, a floating-gate layer and an intergate dielectric layer interposed between the control-gate layer and the floating-gate layer, wherein the intergate dielectric layer has an aluminum oxide layer and a second dielectric material embedded in a surface of the aluminum oxide layer, wherein a dopant material is embedded in the surface of the aluminum oxide layer after a formation of the aluminum oxide layer such as not to disperse the dopant material throughout the aluminum oxide layer, and the dopant material is subsequently treated to form the second dielectric

material, and wherein the dopant material is selected from the group consisting of silicon, zirconium, hafnium and titanium;

a first source/drain region in the substrate adjacent a first sidewall of the gate stack; and

a second source/drain region in the substrate adjacent a second sidewall of the gate stack.

62. The floating-gate field-effect transistor of claim 61, wherein the second dielectric material is a dielectric material selected from the group consisting of oxide forms of silicon, zirconium, hafnium and titanium, and nitride forms of silicon.

63. The floating-gate field-effect transistor of claim 61, wherein the second dielectric material is a dielectric material selected from the group consisting of silicon dioxide, zirconium dioxide, hafnium dioxide, titanium dioxide and silicon nitride.

64. The floating-gate field-effect transistor of claim 61, wherein the aluminum oxide layer is formed by a method selected from the group consisting of thermal evaporation, electron-beam evaporation and ion-beam-assisted deposition.

65. The floating-gate field-effect transistor of claim 64, wherein a degree of porosity of the aluminum oxide layer is controlled during formation of the aluminum oxide layer using a method selected from the group consisting of ion bombardment and plasma activation.

66. The floating-gate field-effect transistor of claim 61, wherein the aluminum oxide layer has a packing density between approximately 0.66 and 0.999.

67. The floating-gate field-effect transistor of claim 61, wherein the dopant material constitutes approximately 0.1% to 30% by weight of the gate dielectric layer.

68. The floating-gate field-effect transistor of claim 61, wherein the aluminum oxide layer has a degree of porosity such that the dopant material embedded in the surface of the aluminum oxide layer constitutes approximately 0.1% to 30% by weight of the gate dielectric layer.

69. The floating-gate field-effect transistor of claim 61, wherein dopant material is formed by blanket depositing the dopant material on the surface of the aluminum oxide layer.

70. The floating-gate field-effect transistor of claim 69, wherein excess dopant material is removed from the surface of the aluminum oxide layer prior to treating the dopant material.

71. The floating-gate field-effect transistor of claim 69, wherein the second dielectric material contains silicon dioxide formed by a chemical vapor deposition of silicon using dilute silane in nitrogen and a substrate temperature of approximately 300°C to 350°C, followed by rapid thermal annealing the silicon in an oxygen-containing atmosphere.

72. The floating-gate field-effect transistor of claim 69, wherein the dopant material is deposited to a thickness less than or equal to an average diameter of the pores.

73. The floating-gate field-effect transistor of claim 61, wherein the floating-gate field-effect transistor is a flash memory cell of a flash memory device.

74. A capacitor, comprising:
a first capacitor plate;
a second capacitor plate; and
a dielectric layer interposed between the first capacitor plate and the second capacitor plate, wherein the dielectric layer includes an aluminum oxide

layer and a second dielectric material embedded in a surface of the aluminum oxide layer, wherein a dopant material is embedded in the surface of the aluminum oxide layer after a formation of the aluminum oxide layer, thereby not dispersing the dopant material throughout the aluminum oxide layer, and the dopant material is subsequently treated to form the second dielectric material, and wherein the dopant material is selected from the group consisting of silicon, zirconium, hafnium and titanium.

75. The capacitor of claim 74, wherein the second dielectric material is a dielectric material selected from the group consisting of oxide forms of silicon, zirconium, hafnium and titanium, and nitride forms of silicon.

76. The capacitor of claim 74, wherein the second dielectric material is a dielectric material selected from the group consisting of silicon dioxide, zirconium dioxide, hafnium dioxide, titanium dioxide and silicon nitride.

77. The capacitor of claim 74, wherein the aluminum oxide layer is formed by a method selected from the group consisting of thermal evaporation, electron-beam evaporation and ion-beam-assisted deposition.

78. The capacitor of claim 77, wherein a degree of porosity of the aluminum oxide layer is controlled during formation of the aluminum oxide layer using a method selected from the group consisting of ion bombardment and plasma activation.

79. The capacitor of claim 74, wherein the aluminum oxide layer has a packing density between approximately 0.66 and 0.999.

80. The capacitor of claim 74, wherein the dopant material constitutes approximately 0.1% to 30% by weight of the gate dielectric layer.

81. The capacitor of claim 74, wherein the aluminum oxide layer has a degree of porosity such that the dopant material embedded in the surface of the aluminum oxide layer constitutes approximately 0.1% to 30% by weight of the gate dielectric layer.

82. The capacitor of claim 75, wherein dopant material is formed by blanket depositing the dopant material on the surface of the aluminum oxide layer.

83. The capacitor of claim 82, wherein excess dopant material is removed from the surface of the aluminum oxide layer prior to treating the dopant material.

84. The capacitor of claim 82, wherein the second dielectric material contains silicon dioxide formed by a chemical vapor deposition of silicon using dilute silane in nitrogen and a substrate temperature of approximately 300°C to 350°C, followed by rapid thermal annealing the silicon in an oxygen-containing atmosphere.

85. The capacitor of claim 82, wherein the dopant material is deposited to a thickness less than or equal to an average diameter of the pores.

86. The capacitor of claim 74, wherein the capacitor is a cell capacitor of a memory cell of a dynamic random access memory device.

87. An electronic system, comprising:
a processor; and
a memory device coupled to the processor;
wherein at least one of the processor and the memory device contain a dielectric layer having a porous aluminum oxide layer and a second dielectric material embedded in pores of the porous aluminum oxide layer;

wherein the second dielectric material is formed of a dopant material selected from the group consisting silicon, zirconium, hafnium and titanium; and

wherein the dopant material is embedded in the pores of the porous aluminum oxide layer after formation of the porous aluminum oxide layer such that the dopant material is not dispersed throughout the porous aluminum oxide layer, and the dopant material is subsequently converted to a dielectric form.